Senior Physical Design Engineer

Responsibilities:

1. In this position you will be leading SoC/Core physical design team working on a range of processor and other IPs and SoCs for applications such as embedded, mobile, cloud, etc.
2. Work on Chip/Block Level Floorplanning, pin assignment. etc.
3. Pre-layout STA to ascertain feasibility, timing constraint validation and feedback to customers and design teams.
4. Review top-level/block-level clock specifications for completeness and feasibility.
5. Lead Physical design tasks (Placement, Timing Optimization, Clock Tree Synthesis, Routing, MMMC, Signoff, DRC/LVS).
6. Lead physical design team to meet aggressive performance power area (PPA) goals with tight project schedules.
7. Perform signoff tasks (RC Extraction, Static Timing Analysis, EM/IR drop analysis and Physical Verification DRC/LVS).
8. Lead and participate in technical and schedule discussions internal and external including with ASIC customers and design teams.

Requirements:

1. MS/BS degree in Electrical, Electronics or Computer Engineering or related field.
2. 5+ years of experience with strong experience in ASIC Physical Design (flat/hierarchical).
3. Experience of SoC multiple tapeouts at 28nm, 16/12/5nm design nodes.
4. Power user of commercial EDA tools from Cadence (Genus, Modus, Innovus, Tempus, QRC, PVS, Voltus, Conformal), or Synopsys (DC, DFT, ICCII/FC, PrimeTime, StarRC, ICV, PrimePower, Formality and RedHawk).
5. Strong knowledge of CPU (RISC-V, Arm), IP/Subsystem, interconnects and industry standard interfaces (USB, DDR, PCIe, UCIe, etc.) from implementation perspective.
6. Strong problem solving skills and ability to analyze and resolve physical design issues related to library, timing constraints or CAD tools is required.
7. Strong experience of Lint, CDC, DFT checking and debugging using Synopsys/Cadence.
8. Strong understanding of ASIC test methodology such as scan insertion, memory BIST and automated test pattern generation (ATPG) will be a plus.
9. Experience with Physical Verification and fixing PV/LVS errors in layout.
10. Expert handling of Verilog HDL based RTL, Netlists, physical design libraries, scripting (Perl/Tcl/Python) is required.
11. Team player with good interpersonal and communication skills.

Aql Tech Solutions

Aql Tech Solutions (Pvt) Limited is a leading commercial provider of a range of RISC-V processor IP cores and solutions targeted for markets, such as datacenters, 5G, edge, AI, mobile, networking, storage, consumer devices and more. Aql Tech Solutions has been founded by industry veterans with strong semiconductor industry experience in the USA and Pakistan.

Aql Tech Solutions (ATS) is based in Islamabad, Pakistan is looking for highly innovative and driven individuals with a passion to work in a professional and high growth environment. Our goals are to develop strong technical talent, skills and to bolster holistic growth of all employees.

We provide a unique career advancement atmosphere, a generous financial package and an opportunity to be part of the highly advanced global semiconductor industry.

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www.aqltechsolutions.com

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